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METHOD AND APPARATUS FOR ERROR DETECTION AND CORRECTION

Abstract of the Disclosure

A Random Access Error Detection and Correction unit (RAEDAC) that incorporates a bit-wise error detection and correction unit (BEDAC) in a memory system. In one embodiment, a word-wise error detection and correction unit (WEDAC) operates in coordination with a BEDAC that performs a bit-wise parity calculation. In another embodiment, a WEDAC operates in coordination with a full bit-wise BEDAC that calculates bit-wise check bits. The RAEDAC may be applied to create a multi-dimensional EDAC where, for example, the memory is partitioned into a stack of planes, and a stack-wise error detection and correction unit (SEDAC) is implemented.